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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,523	11/12/2003	Robert Fu	TRAN-P196	8679

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WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/712,523	FU ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment and Response to Restriction/Election Requirement filed 3/31/05 form the basis of this office action.

Election/Restrictions

Examiner withdraws said election requirement in light of Applicants' comments and acknowledges receipt of the election of the claims 1-14 of Group I invention without traverse.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1-3*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view of Reczek et al (4,798,974). Art disclosed as Prior Art as Admitted by Applicant (APAA) teaches a first control input coupled to a first N-well bias supply line through 150a or 150b (see Figure 2 and page 2, line 18 – 21); and a second control input coupled to a substrate bias supply line through 155a or 155b (see Figure 2 and page 2, line 21 – page 3, line 1).

APAA does not necessarily teach the limitation of "a switched terminal coupled to ground and to the substrate bias supply line and output terminal coupled to a P-type substrate". However, it would have been obvious to include said limitation in view of Reczek et al, who, in a patent on CMOS circuitry with substrate bias supply line (line

from V_{DD} to 16 and from 16 through 17 to substrate: Figure 1) coupled to second control input ('BIAS VOLTAGE GENERATOR" 16, see Figure 1 and col. 4, l. 27-33), hence closely related to APAA (see Reczek et al, title, abstract, col. 1, l. 8-28) teach a switched terminal (electronic switch T4) coupled to ground V_{ss} (loc.cit.) and a switched terminal coupled to said substrate bias supply line (i.e., the electrical line connecting 16 with V_{DD}; loc.cit.) and an output terminal (terminal of 16 on the side of 17) coupled to a P-type substrate (col. 3, l. 17-21), for the specific purpose of discharging potentially damaging powerful currents via additional circuitry (col. 5, l. 14-22). Because both APAA and Reczek et al are relevant during a situation in which a positive supply voltage is switched on (see page 3 of the specification and see Reczek et al, col. 1, l. 29-59) for which Reczek et al provide a remedy as delineated above, there is ample motivation to combine the teaching by Reczek et al with the APAA. All that is needed for the combination is the insertion of said switch between the bias supply line, output terminal and ground, which is straightforward in the art.

On claim 2: said switch is operable in the combined invention to electrically couple said P-type substrate to said ground when a bias voltage is present on said first N-well bias supply line (i.e., line 14 in Reczek et al, cf. col. 3, l. 52-54 and col. 5, l. 14-20).

On claim 3: said switch is operable to electrically couple said P-type substrate to said substrate bias supply line when a substrate bias voltage is present on said substrate bias supply line (loc.cit.) (V_{DD} is the very supply voltage that is switched on, for

which operation the electronic switch T4 is inserted: see col. 1, l. 29-59 and col. 3, l. 52-54).

3. ***Claims 4-8*** are rejected under 35 U.S.C. 103(a) as being unpatentable over APAA and Reczek et al as applied to claim 4 above, and further in view of Nakazato et al (5,386,135). As detailed above, claim 1 is unpatentable over APAA in view of Reczek et al. Neither necessarily claim the further limitations defined by claims 4, 5, 6, 7 or 8. However, it would have been obvious to include said further limitation ad claim 4 as it has long been recognized in the art of CMOS memory devices to provide separate, i.e., independent, bias to their individual N wells (Figure 33) so as to improve the overall breakdown voltage (col. 6, l. 45-61). *Motivation* exists to apply the invention defined by APAA and Reczek et al to any CMOS circuit, in particular to those in semiconductor memory devices in which there are many N-wells as shown by Nakazato et al, wherein the resulting improvement of overall breakdown voltage (loc.cit.) forms an obvious motivation.

On claim 5: in the combined invention said switch is operable to electrically couple said P-type substrate to said ground when a bias voltage is present on said second N-well bias voltage supply line and when it is not present, the relation between the second N-well well bias supply voltage not being of any influence to the switch position by virtue of the independence of the first and second N-well bias voltage supplies as taught by Nakazato et al (loc.cit.).

On claim 6: said switch is operable to electrically couple said P-type substrate to said substrate bias supply line when a substrate bias voltage is present on said

substrate bias supply line (loc.cit.) (V_{DD} is the very supply voltage that is switched on, for which operation the electronic switch T4 is inserted: see col. 1, l. 29-59 and col. 3, l. 52-54).

On claims 7-8: in the combined invention by APAA, Reczek et al and Nakazato et al of which the obviousness was discussed above the voltage of the substrate bias supply line and the N-well bias supply lines are independent because of the independence of the N-well bias supply lines with respect to each other. Therefore, said switch in the combined invention is operable to electrically couple said P-type substrate to either said substrate bias supply line (claim 7) and ground (claim 8) when a substrate bias voltage is present on said substrate and there is no bias voltage present on said N-well line, the substrate bias supply line voltage VDD being an evaluation parameter for operating the switch and the presence or absence of a voltage on the N-well bias line being independent of switch operation, being independent of V_{DD} and ground.

4. ***Claims 9-14*** are rejected under 35 U.S.C. 103(a) as being unpatentable over APAA (loc.cit.) in view of Reczek et al (loc. cit.). Art disclosed as Prior Art as Admitted by Applicant (APAA) teaches:

a first control input coupled to a first N-well bias supply line through 150a or 150b (see Figure 2 and page 2, line 18 – 21);

a second control input coupled to a substrate bias supply line through 155a or 155b (see Figure 2 and page 2, line 21 – page 3, line 1).

APAA does not necessarily teach the limitation of "a switched terminal coupled to ground and a switched terminal coupled to a charge pump enable line; and an output terminal coupled to a P-type substrate".

However, it would have been obvious to include said limitation in view of Reczek et al, who, in a patent on CMOS circuitry with substrate bias supply line (line from V_{DD} to 16 and from 16 through 17 to substrate: Figure 1) coupled to second control input ('BIAS VOLTAGE GENERATOR" 16, see Figure 1 and col. 4, l. 27-33), hence closely related to APAA (see Reczek et al, title, abstract, col. 1, l. 8-28 and Figure 1) teach a switched terminal (electronic switch T4) coupled to ground V_{ss} (loc.cit.), a switched terminal coupled to a charge pump enable line 29 (namely capacitor C built as stack 24/25/26 (cf. col. 3, l. 28-34, col. 4, l. 19-23 and Figure 1) and an output terminal (terminal of 16 on the side of 17) coupled to a P-type substrate (col. 3, l. 17-21), for the specific purpose of discharging potentially damaging powerful currents via additional circuitry (col. 5, l. 14-22). Because both APAA and Reczek et al are relevant during a situation in which a positive supply voltage is switched on (see page 3 of the specification and see Reczek et al, col. 1, l. 29-59) for which Reczek et al provide a remedy as delineated above, there is ample motivation to combine the teaching by Reczek et al with the APAA. All that is needed for the combination is the insertion of said switch between the bias supply line, output terminal and ground, which is straightforward in the art.

On claim 10: said switch is operable in the combined invention to electrically couple said P-type substrate to said ground when a bias voltage is present on said first

N-well bias supply line (i.e., line 14 in Reczek et al, cf. col. 3, l. 52-54 and col. 5, l. 14-20).

On claim 11: said switch is operable to isolate said P-type substrate from ground when an enable signal is present on said charge pump enable line (col. 5, l. 14-20).

On claim 12: the switch by APAA further comprises a second control input coupled to a second N-well bias supply line 150a or 150b (see Figure 2 and page 2, line 18 – 21).

On claims 13-14: said switch in the combined invention is operable to electrically couple (claim 13) and to electrically isolate (claim 14) said P-type substrate to said ground when a bias voltage is present on said second N-well bias supply (said bias voltage is V_{DD}, which is a parameter of evaluation for the switching operation: see Figure 1 and col. 4, l. 14-20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
May 24, 2005

Patent Examiner:
Johannes Mondt (Art Unit: 2826)